

## CLAIMS

What is claimed is:

- 1           1.     A FLASH array comprising:  
2           a plurality of FLASH cells, each FLASH cell comprising a three-dimensional layout  
3           structure where sidewall, top and bottom surfaces of a floating gate include insulating and  
4           conducting films such that electrical parameters of an element of the FLASH cell can be  
5           accurately modeled and controlled.
- 1           2.     The FLASH cell of claim 1 wherein the associated capacitive coupling  
2           factors are modeled accurately between a control gate, a floating gate and the conducting  
3           films.
- 1           3.     The FLASH cell of claim 2 wherein the charge storage may be quantized by  
2           multiple threshold levels.
- 1           4.     The FLASH cell of claim 2 wherein the physical layout of electrodes are  
2           based on proximity effects for the dimensional and shape customizations.
- 1           5.     The FLASH cell of claim 2 wherein the proximity effects provide for the  
2           balanced control-to-floating-gate to bit-line-to-floating-gate capacitance ratios for all cell  
3           operation modes.

- 1           6.     The FLASH cell of claim 2 wherein the proximity effects lead to lower  
2     voltage array operations, power, delay, and stressing advantages.
- 1           7.     The FLASH cell of claim 2 wherein the proximity effects result in array  
2     compact sizes.
- 1           8.     The FLASH cell of claim 2 wherein the proximity effects provide for device  
2     yield and cost advantages.
- 1           9.     The FLASH arrays of claim 1 which includes a SCL circuit for low power  
2     logic peripherals and controls.
- 1           10.    The FLASH arrays of claim 1 which include SCL peripheral circuitry that  
2     utilize 4T SRAMs.
- 1           11.    The FLASH cell of claim 2 which includes SCL peripheral circuitry to form  
2     PLD/FPGA.
- 1           12.    The FLASH cell of claim 2 which includes SCL peripheral circuitry to  
2     provide for use with hardwired or software macros.
- 1           13.    A method of fabricating a FLASH cell comprising the steps of:  
2               forming a plurality of a shallow trenches in a substrate;

3 forming tunnel oxide film above trenches;  
4 etching at least one gate profile in association with the desirable capacitance  
5 coupling ratios;  
6 providing a bit line film and word line film in accordance with desirable  
7 capacitance coupling ratios.

1 14. The method of claim 13 providing the physical layout of electrodes based  
2 upon proximity effects for the dimensional and shape customizer.

1 15. The method of claim 13 wherein the proximity effects provide for the  
2 balanced control-to-floating-gate to bit-line-to-floating-gate capacitance ratios for all cell  
3 operation modes.

1 16. The method of claim 13 wherein the proximity effects lead to lower voltage  
2 array operations, power, delay, and stressing advantages.

1 17. The method of claim 13 wherein the proximity effects result in array compact  
2 sizes.

1 18. The method of claim 13 wherein the proximity effects provide for device  
2 yield and cost advantages.